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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,754	02/02/2001	Ming-Dou Ker	H000039	6902

34003 7590 04/26/2004

INTELLECTUAL PROPERTY SOLUTIONS, INCORPORATED
5717 COLFAX AVENUE
ALEXANDRIA, VA 22311

EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,754	KER ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-11,14 and 16-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,4,7,9,11,14 and 16-18* is/are allowed.

6)☒ Claim(s) *1,3,8 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed February 5, 2004 has been entered and claims 5, 6, 12, 13, 15 and 19 have been cancelled.

Allowable Subject Matter

2. Claims 2, 4, 7, 9, 11, 14 and 16-18 are allowed.

Response to Arguments

3. Applicants' arguments filed February 5, 2004 have been fully considered but they are not persuasive. Applicants argue that the references of record do not read into claims 1, 3, 8 and 10. Specifically, Ker et al. ("Ker") USPN 6,566,715/Lee et al. ("Lee") USPN 6,097,066 do not teach or fairly suggest that a fourth region of a first conductivity or P+ type is disposed between a second region of a first MOS transistor and a third region of a second MOS transistor or between a source region of a first MOS transistor and a source region of a second MOS transistor.

4. In response to applicants' arguments that Ker does not teach or fairly suggest that a fourth region of a first conductivity or P+ type is disposed between a second region of a first MOS transistor and a third region of a second MOS transistor, Ker discloses in fig. 5 a fourth region 40 of a first conductivity or P+ type being disposed not only between region 36 of a first MOS transistor and region 36 of a second MOS transistor but also between region 38 first MOS transistor and region 38 of a second MOS transistor.

5. In response to applicants' arguments that Lee does not teach or fairly suggest that a fourth region of a first conductivity or P+ type is disposed between a second region of a first MOS transistor and a third region of a second MOS transistor, Lee discloses in figs. 5 and 6 a fourth region 550 of the first conductivity type being disposed between a second region 530 of a first MOS transistor and a third region 530 of a second MOS transistor. Examiner would also like to point out that item 4 of the previous Office Action does not describe region 550 as being disposed between drains 510, rather it explicitly describes region 550 as being disposed between source regions 530.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

7. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Ker USPN 6,566,715.

Ker et al discloses in figs. 5 and 11 a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a substrate of a first conductivity type forming a base for said semiconductor structure; a first region 36 of a second conductivity type within said substrate for forming a drain of a first MOS

transistor; a second region 38 of the second conductivity type within said substrate for forming a source of the first MOS transistor; a third region 36 of the second conductivity type for forming a source of a second MOS transistor, wherein a fourth region 40 of the first conductivity type is disposed between the second region of said first MOS transistor and the third region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor.

Regarding claim 3, Ker discloses a pre-buffer circuit 70 coupled to a gate of the first MOS transistor Mn3; and an outpad 68 coupled to said first region of the first MOS transistor.

8. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Lee USPN 6,097,066.

Lee discloses in fig. 6 a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a substrate of a first conductivity type forming a base for said semiconductor structure; a first region 510 of a second conductivity type within said substrate for forming a drain of a first MOS transistor; a second region 530 of the second conductivity type within said substrate for forming a source of the first MOS transistor; a third region 530 of the second conductivity type for forming a source of a second MOS transistor, wherein a fourth region 550 of the first conductivity type is disposed between the second region of said first MOS transistor and the third region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor.

9. Claims 8 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Ker USPN 6,566,715.

Ker discloses in figs. 5 and 11 a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a p-type substrate of forming a base for said semiconductor structure; a first N+ region 36 within said substrate for forming a drain of a first MOS transistor; a second N+ region 38 within said substrate for forming a source of the first MOS transistor; a third N+ region 36 within said substrate for forming a source of a second MOS transistor, wherein a P+ region 40 is disposed between the second N+ region of said first MOS transistor and the third N+ region of the second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor.

Regarding claim 10, Ker discloses a pre-buffer circuit 70 coupled to a gate of the first MOS transistor Mn3; and an outpad 68 coupled to said first region of the first MOS transistor.

10. Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Lee USPN 6,097,066.

Lee discloses in fig. 5 a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a p-type substrate of forming a base for said semiconductor structure; a first N+ region 510 within said substrate for forming a drain of a first MOS transistor; a second N+ region 530 within said substrate for forming a source of the first MOS transistor; a third N+ region 530 within said substrate for forming a source of a second MOS transistor, wherein a P+ region 550 is disposed between the second N+ region of said first MOS transistor and the third N+ region of the second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ikehashi et al. USPN 6,320,231 disclose a device for protecting a chip from damage due to ESD.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
April 15, 2004

Minhloan Tran
Primary Examiner
Art Unit 2826